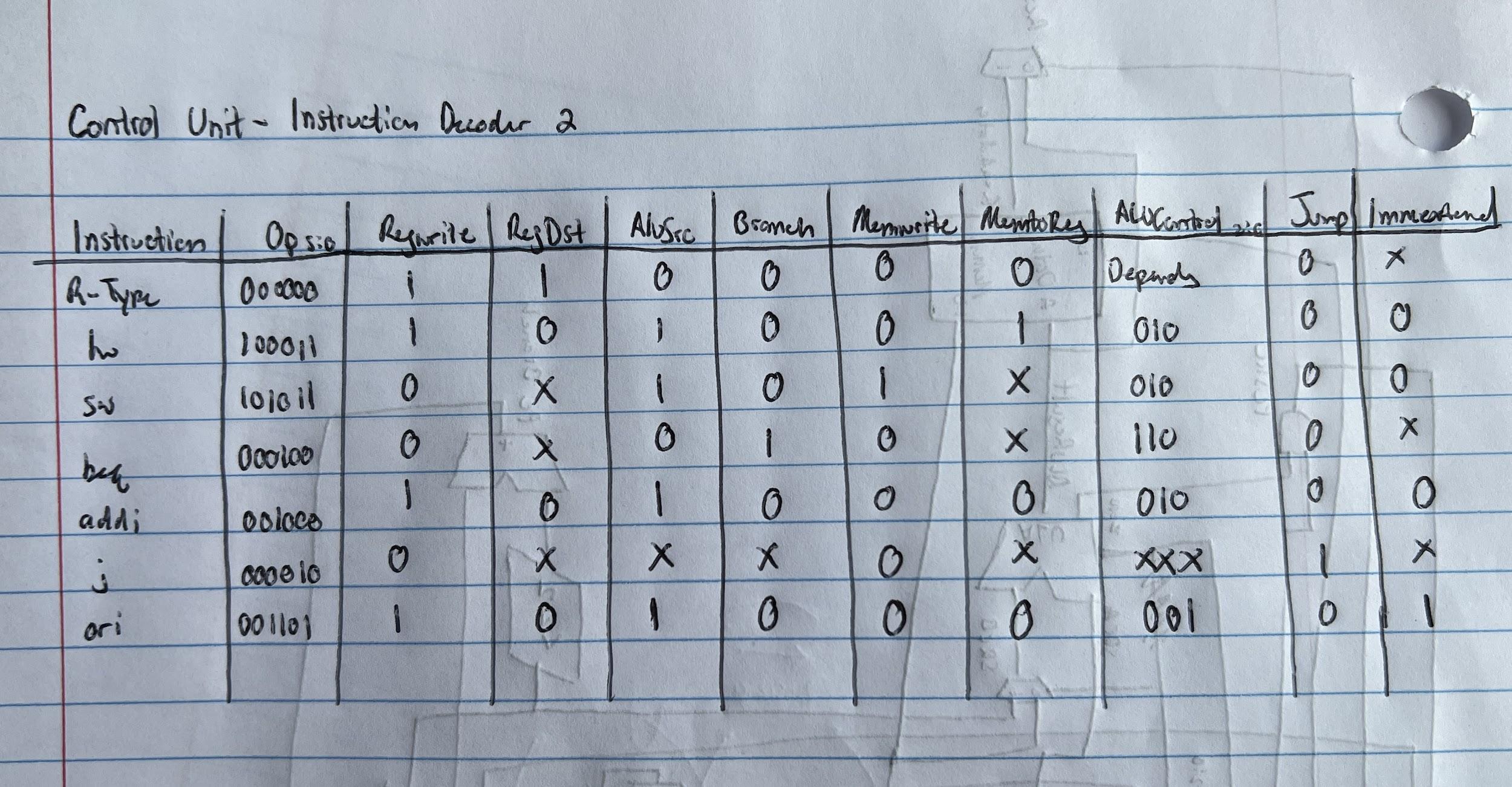
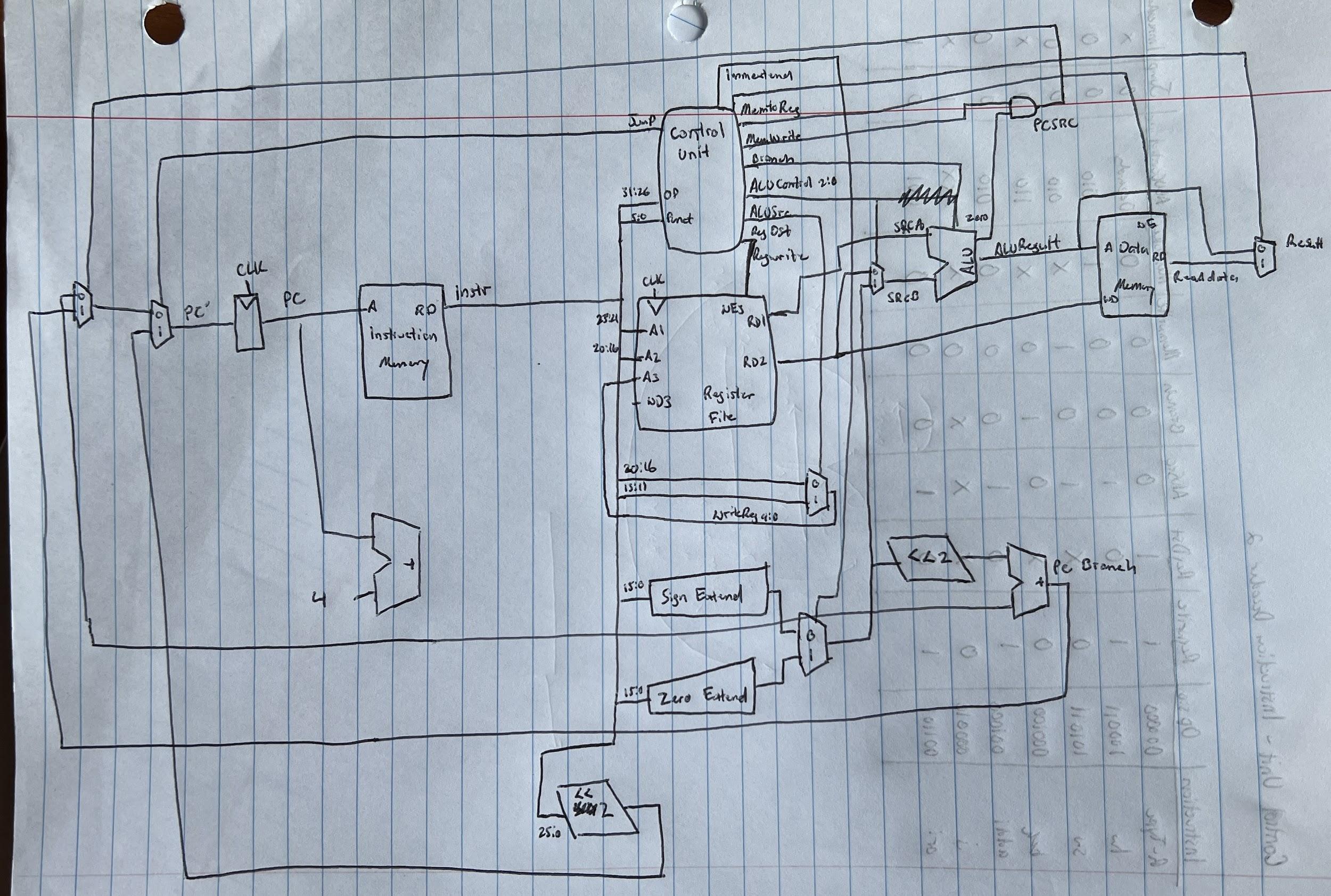
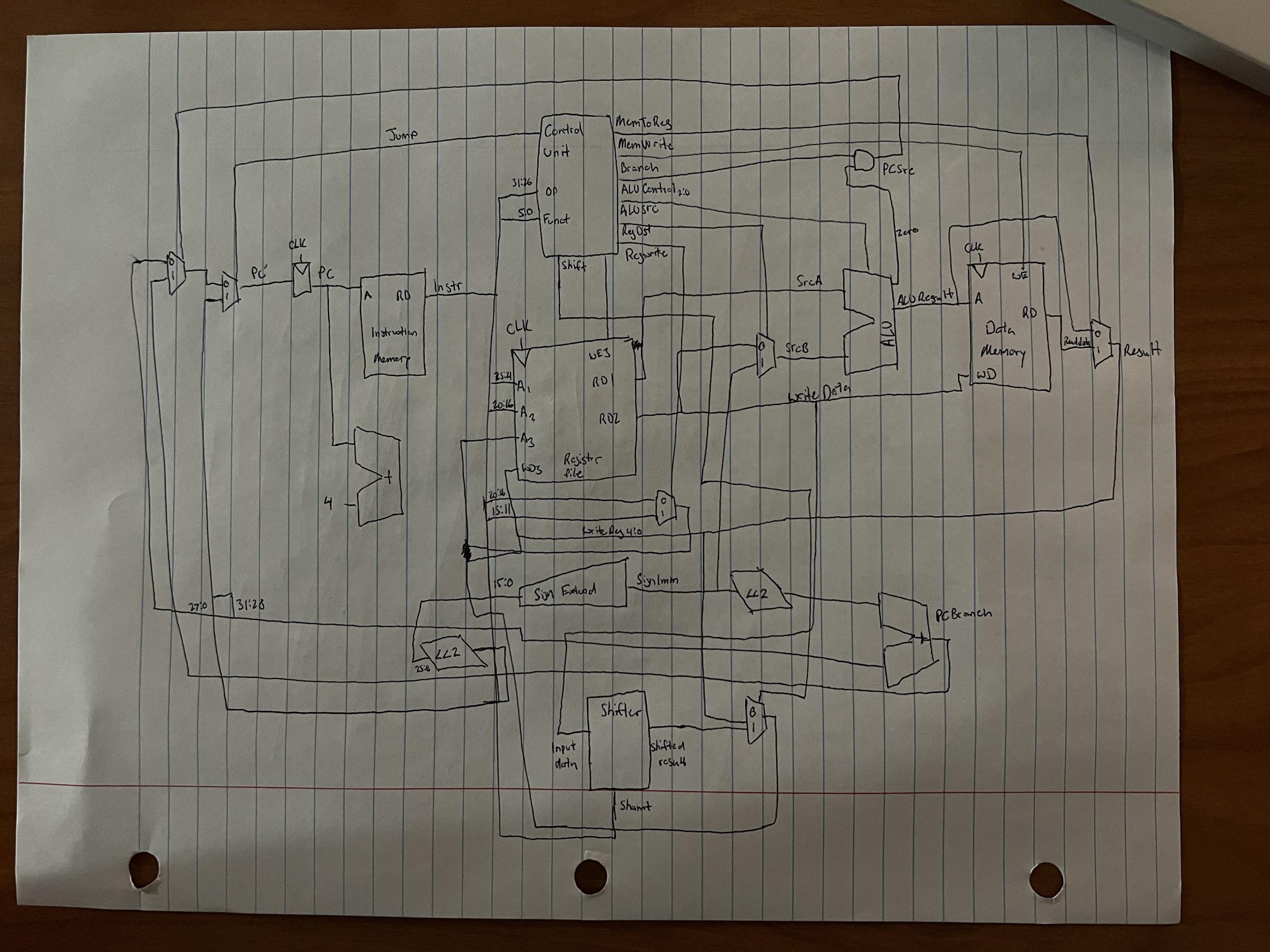
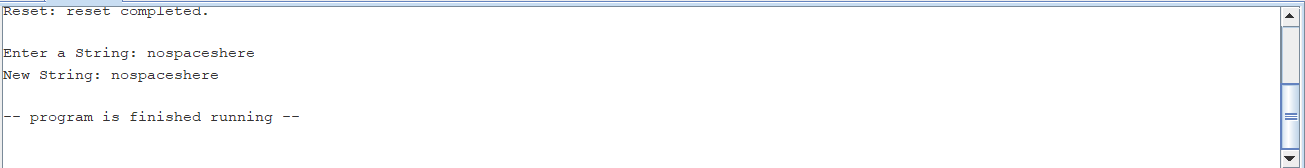
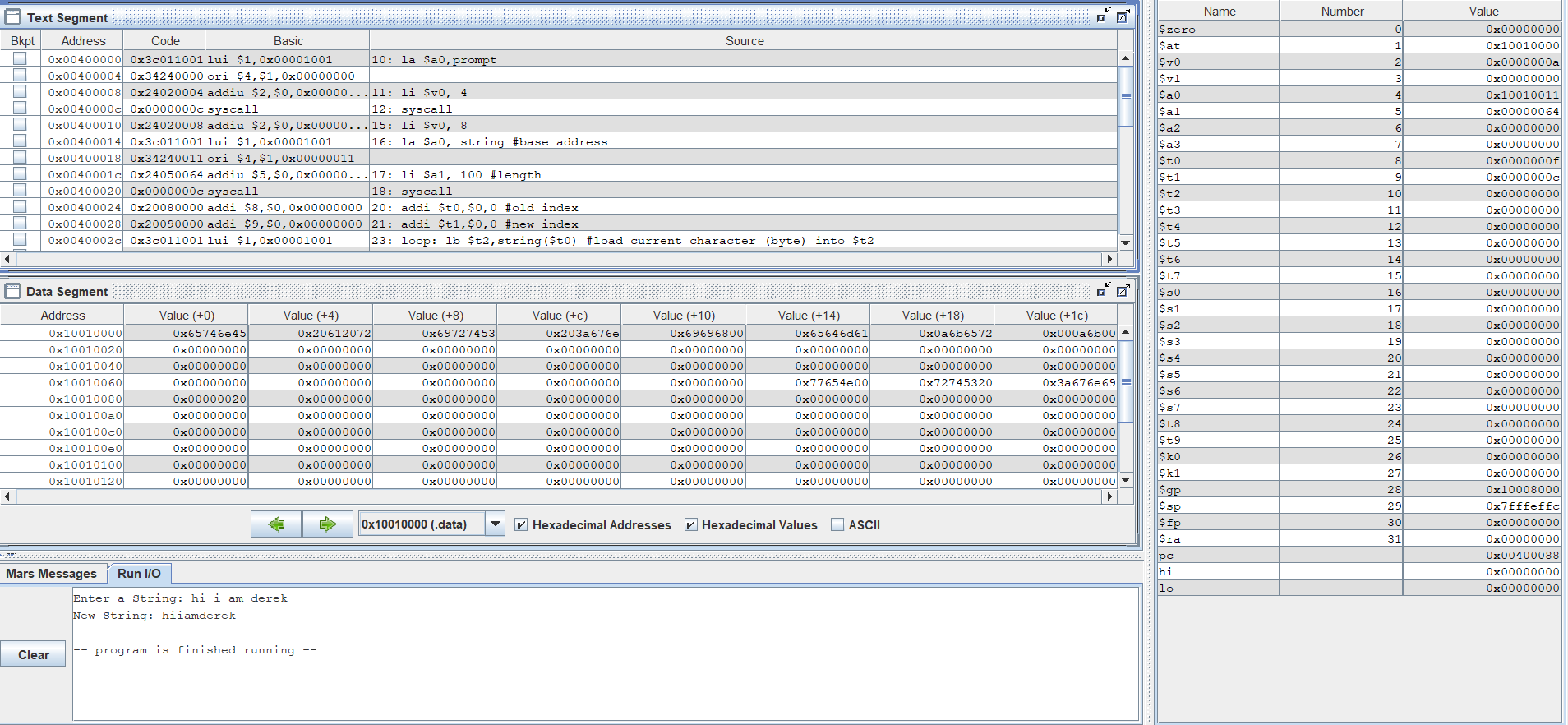
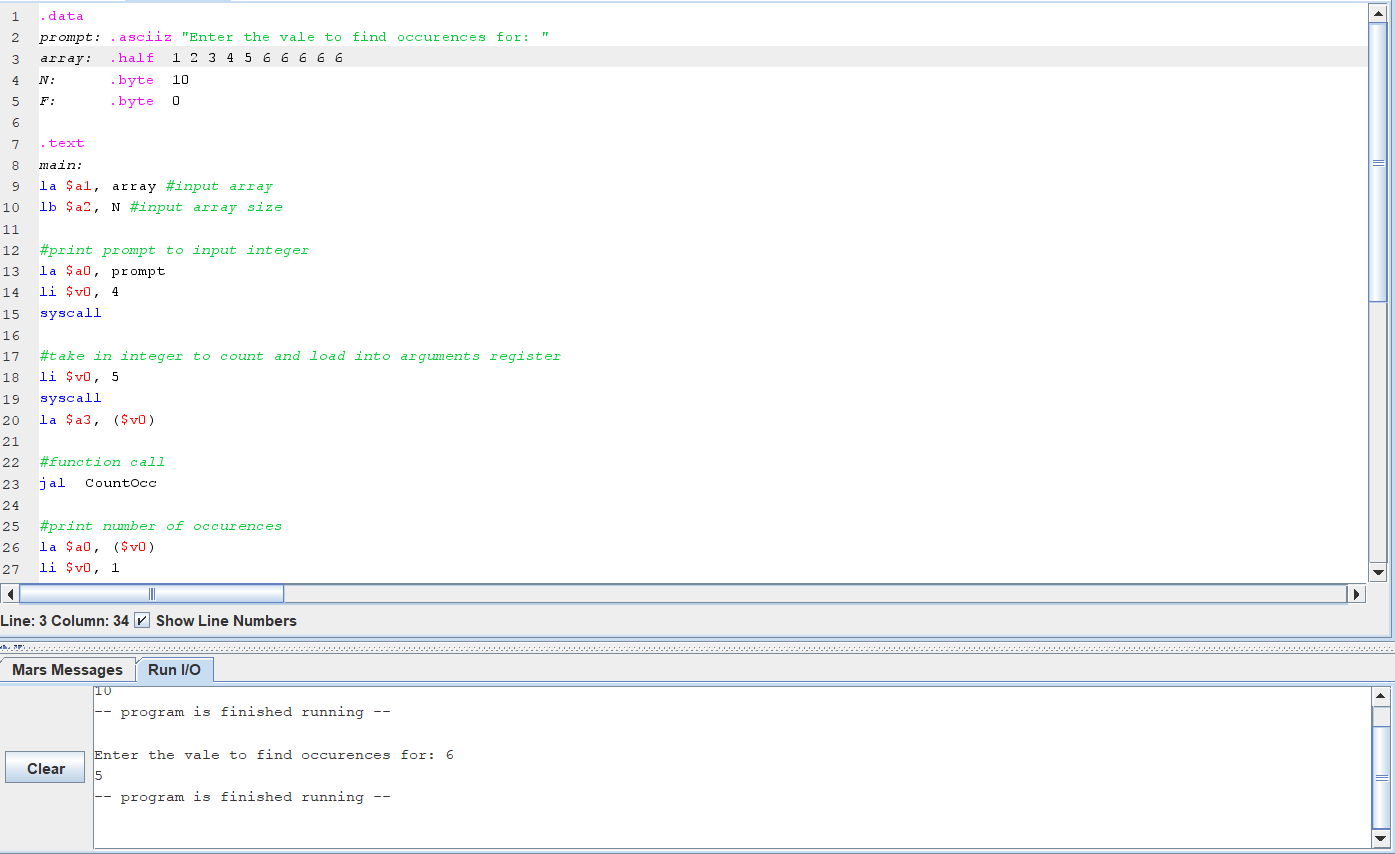
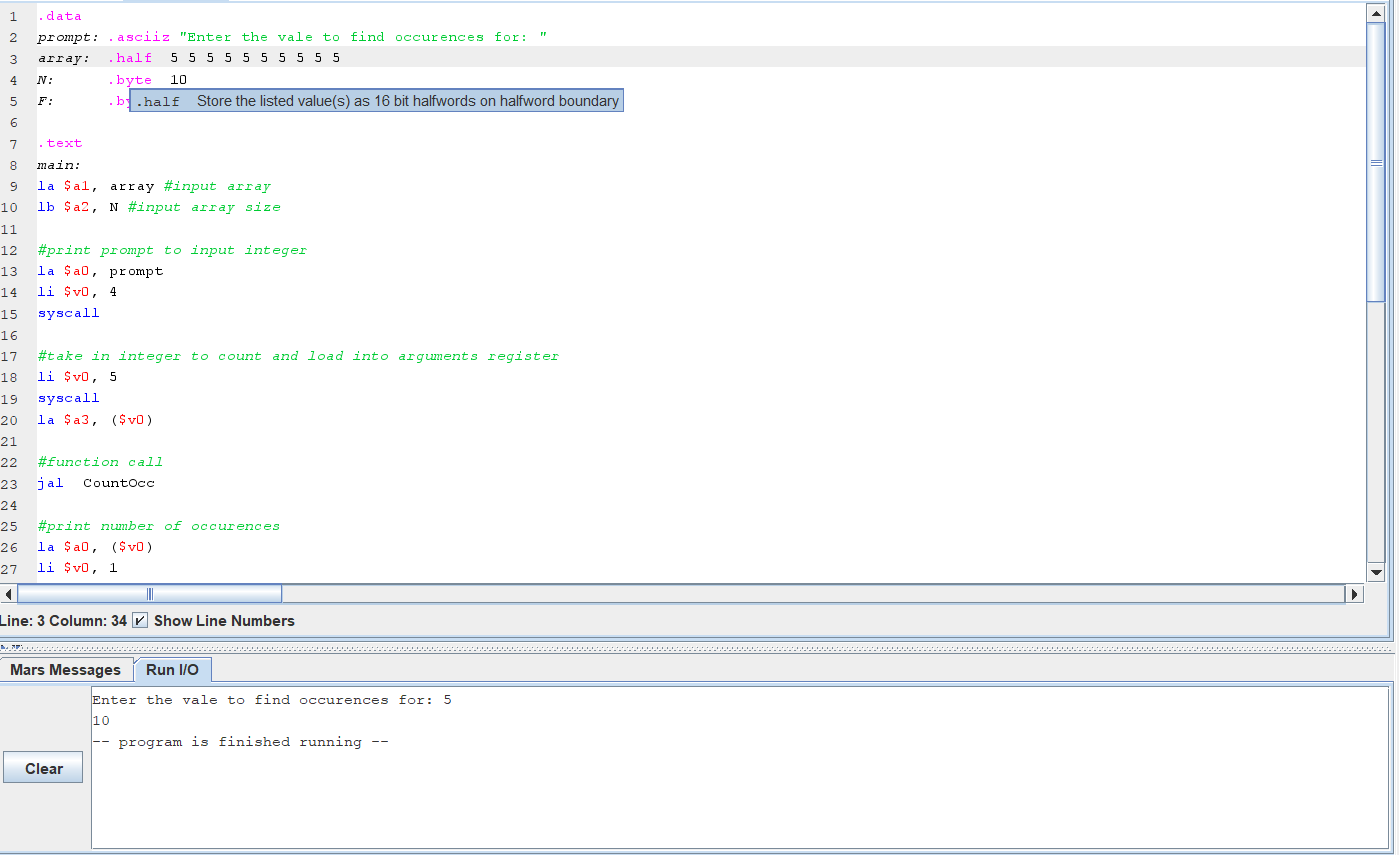
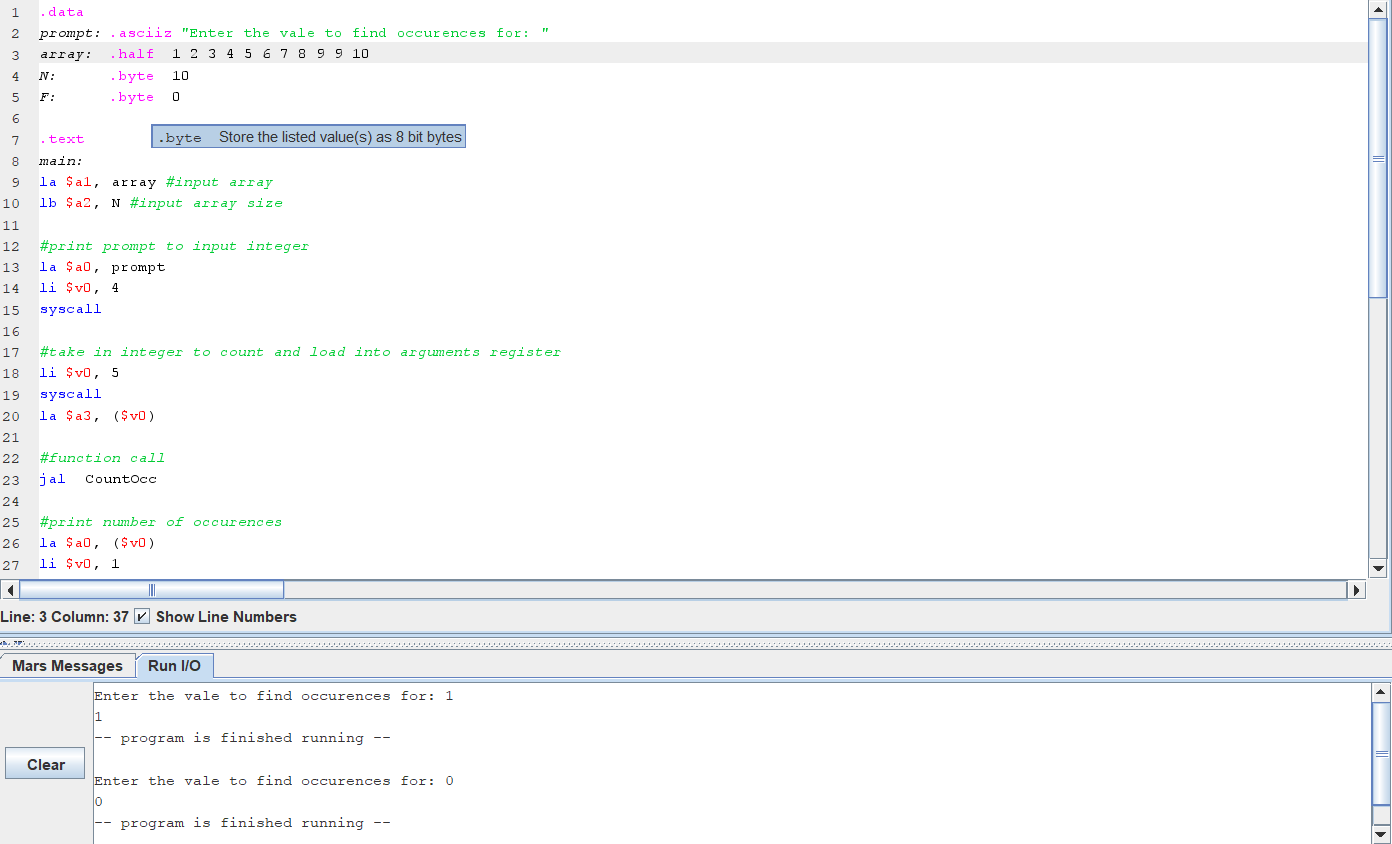
1. -



1. 
   1. (In case this is hard to read: it is the same circuit except there is a shifter and multiplexer added. The shifter get its input from ReadData2 and outputs its shifted result to the 1 input for the multiplexer. The shamt is derived from Instr. The multiplexer’s 0 input is from Result and it outputs to WD3 in the register file. Its select is from the control unit.
2. -
   1. T\_add = t\_pcqPC + t\_mem + t\_RF + t\_mux + t\_ALU + t\_mux + t\_RF = t\_pcqPC + t\_mem + 2t\_RF + 2t\_mux + t\_ALU = 30 + 250 + 2(150) + 2(25) + 200 = 830 ps
   2. t\_pcqPC + t\_mem + t\_RF + t\_mux + t\_ALU + t\_mem = t\_pcqPC + 2t\_mem + t\_RF + t\_mux + t\_ALU = 30 + 2(250) + 150 + 30 + 200 = 910 ps
3. 

—----------------------------------------------------------------------------------------------------------------------------

1. 

—--------------------------------------------------------------------------------------------------------------------------

1. 